REMARKS

Pending Claims

Claim 164 has been amended to overcome the 35 U.S.C. §112, second paragraph rejection. In particular, claim 164 sets forth that the time interval is set to N multiplication of a predetermined unit time. Further, the unit time is now claimed as being common to all of the plurality of processing apparatuses and the inter-apparatus transporter. As amended, claim 164 complies with 35 U.S.C. §112, second paragraph, and therefore the rejection should be withdrawn. New claims 165-169 have been drafted in compliance with 35 U.S.C. §112.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority.

Specification

The Abstract has been amended, as required. Attached is the marked-up Abstract of the Disclosure.

35 U.S.C. §103

Claim 164 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Nishida et al (Nishida), U.S. Patent No. 5,436,848. Applicants request reconsideration of the rejection and further assert that all of pending claims 164-169 are patentable over Nishida and remainder of the art of record.

According to one aspect of the present invention a fabricating method for semiconductor wafers is provided wherein a plurality of processing apparatuses each including at least one processing chamber and an interface having transporting means are interconnected by an inter-apparatus transporter. The inter-apparatus transporter and each of the processing apparatuses are assigned a time interval. The time interval for each processing apparatus includes the time required for transporting a semiconductor wafer to be processed into the processing chamber at the interface, the time required for processing the semiconductor wafer in the processing chamber, and the time required for transporting the semiconductor wafer out of the processing chamber out to the interface. The time intervals for the inter-apparatus

transporter and the processing apparatuses are set to N multiplication of a predetermined unit of time that is common to all of the plurality of the processing apparatuses and the inter-apparatus transporter. N is a positive integer, and the unit of time is set forth as being longer than the shortest required time for either processing in each of the processing chambers or for transporting with the inter-apparatus transporter, but shorter than the longest required time for either processing in each of the processing apparatuses or for transporting with the inter-apparatus transporter.

According to the present invention, therefore, the sequence of processes in a fabricating method including processing semiconductor wafers by a plurality of processing apparatuses, can be determined efficiently even when several processing apparatuses are used in the fabrication method. Further, because the inter-apparatus transporter is used for connecting the processing apparatuses, the waiting time between two processes is reduced as compared with a conventional fabricating system in that the inter-apparatus transporter is also assigned a time interval that is N multiplication of the predetermined unit of time. In this

way, the fabricating method for the whole fabricating system can be managed efficiently.

In the processing of semiconductor wafers disclosed by Nishida, the problem of different cycle times among different apparatuses or processes is addressed. In particular, the cycle time of the processes affects the waiting time to be included in the transporting of the semiconductor wafers from one process to the next. To overcome this problem, Nishida discloses driving the robot 5, which transports the semiconductor wafers, according to a single constant cycle time. The cycle time that is chosen is that of the longest process, e.g. 70^{s} in the preferred embodiment disclosed by Nishida. In order to control the processing according to Nishida, wafers are transported between processes in a predetermined amount of time, then a waiting time is provided so that transporting of the wafers between processes is conducted within the cycle time. Accordingly, Nishida does not disclose assigning a time interval that is set to N multiplication of a predetermined unit time that is common to all of the plurality of processing apparatuses and the inter-apparatus transporter as in the present invention.

Further, as set forth in claim 164, the unit time is longer than the shortest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter, but shorter than the longest required time for either processing in each of the processing apparatus or for transporting by the inter-apparatus transporter. In claim 168, the time unit that is common to all of the plurality of processing apparatuses is longer than the shortest required time for processing a semiconductor wafer in each of the processing chambers, but shorter than the longest required time for processing in each of the processing chambers. Further, in claim 169, the predetermined unit time that is common to all of the plurality of processing apparatuses is as set forth in claim 164, with the additional limitation that the time interval between setting of a semiconductor wafer at the interface of one of the processing apparatuses by the inter-apparatus transporter and setting at the interface of another processing apparatus is set to M multiplication of the predetermined unit time, wherein M is a positive integer. Nishida neither discloses nor suggests

these aspects of the claimed combination of the invention and therefore the 35 U.S.C. §103(a) rejection should be withdrawn.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination is requested.

Respectfully submitted,

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